# ShiftsReduce: Minimizing Shifts in Racetrack Memory 4.0

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#### Abstract

Racetrack memories (RMs) have significantly evolved since their conception in 2008, making them a serious contender in the field of emerging memory technologies. Despite key technological advancements, the access latency and energy consumption of an RM-based system are still highly influenced by the number of *shift* operations. These operations are required to move bits to the right positions in the racetracks. This paper presents data placement techniques for RMs that maximize the likelihood that consecutive references access nearby memory locations at runtime thereby minimizing the number of shifts. We present an *integer linear programming* (ILP) formulation for optimal data placement in RMs, and revisit existing offset assignment heuristics, originally proposed for random-access memories. We introduce a novel heuristic tailored to a realistic RM and combine it with a genetic search to further improve the solution. We show a reduction in the number of shifts of up to 52.5%, outperforming the state of the art by up to 16.1%.

## 1 Introduction

Conventional SRAM/DRAM-based memory systems are unable to conform to the growing demand of low power, low cost and large capacity memories. Increase in the memory size is barred by technology scalability as well as leakage and refresh power. As a result, multiple non-volatile memories such as *phase change memory* (PCM), *spin transfer torque* (STT-RAM) and *resistive RAM* (ReRAM) have emerged and attracted considerable attention [1–4]. These memory technologies offer power, bandwidth and scalability features amenable to processor scaling. However, they pose new challenges such as imperfect reliability and higher write latency. The relatively new spin-orbitronics based *racetrack memory* (RM) represents a promising option to surmount the aforementioned

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Table 1: Comparison of RM with other memory technologies [6, 12]

	SRAM	eDRAM	DRAM	STT-RAM	ReRAM	PCM	RaceTrack 4.0
Cell Size $(F^2)$	120-200	30-100	4-8	6-50	4-10	4-12	$\leq 2$
Write Endurance	$\geq 10^{16}$	$\geq 10^{16}$	$\geq 10^{16}$	4 X 10 <sup>12</sup>	10 <sup>11</sup>	10 <sup>9</sup>	10 <sup>18</sup>
Read Time	Very Fast	Fast	Medium	Medium	Medium	Slow	Fast
Write Time	Very Fast	Fast	Medium	Slow	Slow	Very Slow	Fast
Dynamic Write Energy	Low	Medium	Medium	High	High	High	Low
Dynamic Read Energy	Low	Medium	Medium	Low	Low	Medium	Low
Leakage Power	High	Medium	Medium	Low	Low	Low	Low
Retention Period	As long as	$30 - 100 \ \mu s$	64 - 512  ms	Variable	Years	Years	Years
	volt applied						

limitations by offering ultra-high capacity, energy efficiency, lower per bit cost, higher reliability and smaller read/write latency [5,6]. Due to these attractive features, RMs have been investigated at all levels in the memory hierarchy. Table 1 provides a comparison of RM with contemporary volatile and non-volatile memories.

The diverse memory landscape has motivated research on hardware and software optimizations for more efficient utilization of NVMs in the memory subsystem. To avoid the design complexity added by hardware solutions, softwarebased data placement has become an important emerging area for compiler optimization [7]. Even modern days processors such as intel's Knight Landing Processor offer means for software managed on-board memories. Compiler guided data placement techniques have been proposed at various levels in the memory hierarchy, not only for improving the temporal/spatial locality of the memory objects but also the lifetime and high write latency of NVMs [8–11]. In the context of *near data processing* (NDP), efficient data placement improves the effectiveness of NDP cores by allowing more accesses to the local memory stack and mitigating remote accesses.

In this paper, we study data placement optimizations for the particular case of racetrack memories. While RMs do not suffer from reliability and latency issues, they pose a significantly different challenge. From the architectural perspective, RMs store multiple bits -1 to 100— per access point in the form of magnetic domains in a tape-like structure, referred to as track. Each track is equipped with one or more magnetic tunnel junction (MTJ) sensors, referred to as access ports, that are used to perform read/write operations. While a track could be equipped with multiple access ports, the number of access ports per track are always much smaller than the number of domains. In the scope of this paper, we consider the ideal single access port per track for ultra high density of the RM. This implies that the desired bits have to be shifted and aligned to the port positions prior to their access. The shift operations not only lead to variable access latency but also impact the energy consumption of a system, since the time and the energy required for an access depend on the position of the domain relative to the access port. We propose a set of techniques that reduce the number of shift operations by placing temporally close accesses at nearby locations inside the RM.

Concretely, we make the following contributions.

- 1. An *integer linear programming* (ILP) formulation of the data placement problem for RMs.
- 2. A thorough analysis of existing offset assignment heuristics, originally proposed for data placement in DSP stack frames, for data placement in RM.
- 3. *ShiftsReduce*, a heuristic that computes memory offsets by exploiting the temporal locality of accesses.
- 4. An improvement in the state-of-the-art RM-placement heuristic [13] to judiciously decide the next memory offset in case of multiple contenders.
- 5. A final refinement step based on a genetic algorithm to further improve the results.

We compare our approach with existing solutions on the OffsetStone benchmarks [14]. ShiftsReduce diminishes the number of shifts by 28.8% which is 4.4% and 6.6% better than the best performing heuristics [14] and [13] respectively.

The rest of the paper is organized as follows. Section 2 explains the recently proposed RM 4.0, provides motivation for this work and reviews existing data placement heuristics. Our ILP formulation and the ShiftsReduce heuristic are described in Section 3 and Section 4 respectively. Benchmarks description, evaluation results and analysis are presented in Section 5. Section 6 discusses state-of-the-art and Section 7 concludes the paper.

# 2 Background and motivation

This section provides background on the working principle of RMs, current architectural sketches and further motivates the data placement problem (both for RAMs and RMs).

#### 2.1 Racetrack memory

Memory devices have evolved over the last decades from hard disk drives to novel spin-orbitronics based memories. The latter uses spin-polarized currents to manipulate the state of the memory. The domain walls (DWs) in RMs are moved into a third dimension by an electrical current [5,15]. The racetracks can be placed vertically (3D) or horizontally (2D) on the surface of a silicon wafer as shown in Fig. 1. This allows for higher density but is constrained by crucial design factors such as the shift speed, the DW-to-DW distance and insensitivity to external influences such as magnetic fields.

In earlier RM versions, DWs were driven by a current through a magnetic layer which attained a DW velocity of about 100 ms<sup>-1</sup> [16]. The discovery of even higher DW velocities in structures where the magnetic film was grown on top of a heavy metal allowed to increase the DW velocity to about 300 ms<sup>-1</sup> [17]. The driving mechanism is based on spin-orbit effects in the heavy metal which lead to spin currents injected into the magnetic layer [18]. However, a major



Figure 1: Racetrack horizontal and vertical placements ( $I_{sl}$  and  $I_{sr}$  represent left and right shift currents respectively)

drawback of these designs was that the magnetic film was very sensitive to external magnetic fields. Furthermore, they exhibited fringing fields which did not allow to pack DWs closely to each other.

The most recent RM 4.0 resolved these issues by adding an additional magnetic layer on top, which fully compensates the magnetic moment of the bottom layer. As a consequence, the magnetic layer does not exhibit fringing fields and is insensitive to external magnetic fields. In addition, due to the exchange coupling of the two magnetic layers, the DWs velocity can reach up to 1000 ms<sup>-1</sup> [6, 19].



Figure 2: Racetrack memory architecture [20]

#### 2.1.1 Memory architecture

Fig. 2 shows a widespread architectural sketch of an RM based on [20]. In this architecture an RM is divided into multiple *Domain Block Clusters* (*DBCs*),

each of which contains M tracks with N DWs each. Each domain wall stores a single bit, and we assume that each M-bit variable is distributed across Mtracks of a DBC. Accessing a bit from a track requires shifting and aligning the corresponding domain to the track's port position. We further assume that the domains of all tracks in a particular DBC move in a lock step fashion so that all M bits of a variable are aligned to the port position at the same time for simultaneous access. We consider a single port per track because adding more ports increases the area. This is due to the use of additional transistors, decoders, sense amplifiers and output drivers. As shown in Fig. 2, each DBC can store a maximum of N variables.

Under the above assumptions, the shift cost to access a particular variable may vary from 0 to N - 1. It is worth to mention that worst case shifts can consume more than 50% of the RM energy [21] and prolong access latency by 26x compared to SRAM [20]. The architectural simulator, RTSim [22], can be used to analyze the shifts' impact on the RM performance and energy consumption, and explore its design space by varying the above mentioned design parameters.



Figure 3: Motivation example

#### 2.2 Motivation example

To illustrate the problem of data placement consider the set of data items and their access order from Fig. 3a. We refer to the set of program data items as the set of program variables  $(\mathcal{V})$  and the set of their access order as access sequence (S), where  $S_i \in \mathcal{V} \ \forall i \in \{0, 1, \ldots, |S|-1\}$ , for any given source code. Note that data items can refer to actual variables placed on a function stack or to accesses to fields of a structure or elements of an array. We assume two different, a naive (P1) and a more carefully chosen (P2), memory placements of the program variables as shown in Fig. 3b.

The number of shifts for the two different placements, P1 and P2 in Fig. 3b, are shown in Fig. 4. The shift cost between any two successive accesses in the access sequence is equivalent to the absolute difference of their memory offsets (e.g, |2 - 4| for b,c in P1). The naive data placement P1 incurs 51 shifts in accessing the entire access sequence, while P2 incurs only 19, i.e.,  $2.6 \times$  better.

	b	c	a	e	f	d	a	c	e	d	a	c	a	d	e	f
P1	→ 2	2 4	4	1 2	2 2	2 5	5 4	4 3	3 4	4 :	5 4	4 4	1 5	5 4	1 2	261
P2	<b>→</b> ]	1	1 2	2	1 2	2	1	1 3	3	1	1	1	1 1	l 1	1	1 🕦

Figure 4: Number of shifts in placements P1 and P2 from Fig 3b (encircled numbers show the total shift cost)

This leads to an improvement in both latency and energy consumption for the simple illustrative example.



Figure 5: Data placement in RMs

### 2.3 Problem definition

Fig. 5 shows a conceptual flow of the data placement problem in RMs. The access sequence corresponds to memory traces which can be obtained with standard techniques. They can be obtained via profiling and tracing, e.g., using Pin [23], inferred from static analysis, e.g., for *Static Control Parts* using polyhedral analysis, or with a hybrid of both as in [24]. In this paper we assume the traces are given and focus on the data placement step to produce the memory layout. We investigate a number of exact/inexact solutions that intelligently decide *memory offsets of the program variables referred to as memory layout* based on the access sequence. The memory for which the layout is generated could either be a scratchpad memory, a software managed flat memory similar to the on-board memory in intel's Knight Landing Processor or the memory stack exposed to an NDP core.

The shift cost of an access sequence depends on the memory offsets of the data items. We assume that each data item is stored in a single memory offset of the RM (cf. Section 2.1.1). We denote the memory offset of a data item  $u \in \mathcal{V}$  as  $\beta(u)$ . The shift cost between two data items u and v is then:

$$\Delta(u, v) = |\beta(u) - \beta(v)| \quad \forall u, v \in \mathcal{V}$$
(1)

The total shift cost (C) of an access sequence (S) is computed by accumulating the shift costs of successive accesses:

$$C = \left(\sum_{i=0}^{|S|-2} \Delta(S_i, S_{i+1})\right) \tag{2}$$

The data placement problem for RMs can be then defined as:

**Definition 1** Given a set of variables  $\mathcal{V} = \{v_0, v_1, \dots, v_{n-1}\}$  and an access sequence  $S = (S_0, S_1, \dots, S_{m-1}), S_i \in \mathcal{V}$ , find a data placement  $\beta$  for  $\mathcal{V}$  such that the total cost C is minimized.

#### 2.4 State-of-the-art data placement solutions

The data placement problem in RMs is similar to the classical single offset assignment (SOA) problem in DSP's stack frames [14, 25–27]. The heuristics proposed for SOA assign offsets to stack variables; aiming at maximizing the likelihood that two consecutive references at runtime will be to the same or adjacent stack locations. Most SOA heuristics work on an *access graph* and formulate the problem as maximum weighted Hamiltonian path (MWHP) or maximum weight path covering (MWPC). An access graph G = (V, E) represents an access sequence where V is the set of vertices corresponding to program variables ( $\mathcal{V}$ ). An edge  $e = \{u, v\} \in E$  has weight  $w_{uv}$  if variables  $u, v \in \mathcal{V}$  are accessed consecutively  $w_{uv}$  times in S. The assignment is then constructed by solving the MWHP/MWPC problem. The access graph for the access sequence in Fig. 3a is shown in Fig. 6.

The SOA cost for two consecutive accesses is *binary*. That is, if the next access cannot be reached within the auto-increment/decrement range, an extra instruction is needed to modify the address register (cost of 1). The cost is 0 otherwise. In contrast, the shift cost in RM is a natural number. For RM-placement, the SOA heuristics must be revisited since they only consider edge weights of successive elements in S. This may produce better results on small access sequences due to the limited number of vertices and smaller end-to-end distance in S, but might not perform well on longer access sequences. In this paper, we extend the SOA heuristics to account for the more general cost function.



Figure 6: Access graph for the access sequence in Fig. 3a

Chen et al. recently proposed a group-based heuristic for data placement in RMs [13]. Based on an access graph it assigns offsets to vertices by moving them to a group g. The position of a data item within a group indicates its memory offset. The first vertex added to the group has the maximum *vertex-weight* in the access graph where vertex-weight is the sum of all edge weights that connect a vertex to other vertices in G. The remaining elements are iteratively added to

the group, based on their vertex-to-group weights (maximum first). The vertexto-group weight of a vertex u is the sum of all edge weights that connect u to the vertices in g.

We argue that intelligent tie-breaking for equal vertex-to-group weights deserves investigation. Further the static assignment of highest weight vertex to offset 0 seems restrictive. Defining positions relative to other vertices provides more flexibility to navigate the solution space.

# 3 Optimal data placement: ILP formulation

This section presents an ILP formulation for the data placement problem in RM. Consider the access graph G and the access sequence S to variables  $v \in \mathcal{V}$ , the edge weight  $w_{v_iv_j}$  between variables  $v_i, v_j$  can be computed as:

$$w_{v_i v_j} = \begin{cases} \sum_{x=0}^{m-2} \Upsilon_{ix} \cdot \Upsilon_{j,x+1} + \Upsilon_{jx} \cdot \Upsilon_{i,x+1}, & i \neq j \\ 0, & i = j \end{cases}$$
(3)

with  $i, j \in \{0, 1, .., n - 1\}, n = |\mathcal{V}|, m = |S|$  and  $\Upsilon$  defined as:

$$\Upsilon_{ix} = \begin{cases} 1, & \text{if } S_x = v_i \\ 0, & \text{otherwise} \end{cases}$$
(4)

To model unique variable offsets we introduce binary variables  $(\Theta_{io})$ :

$$\Theta_{io} = \begin{cases} 1, & \text{if } v_i \text{ has memory offset } o, \ \forall i, o \in \{0, 1, .., n-1\} \\ 0, & \text{otherwise} \end{cases}$$
(5)

The memory offset of  $v_i$  is then computed as:

$$\beta(v_i) = \sum_{o=0}^{n-1} \Theta_{io} \cdot o \tag{6}$$

Since edges in the access graph embodies the access sequence information, we use them to compute the total shift cost as:

$$C = \left(\sum_{i=0}^{n-1} \sum_{j=i+1}^{n-2} w_{v_i v_j} \cdot \Delta(v_i, v_j)\right)$$
(7)

The cost function in Equation 7 is not inherently linear due to the absolute function in  $\Delta(v_i, v_j)$  (cf. Equation 1). Therefore, we generate new products and perform subsequent linearization. We introduce two integer variables  $(p_{ij}, q_{ij}) \in \mathbb{Z}$  to rewrite  $|\beta(v_i) - \beta(v_j)|$  as:

$$\Delta(v_i, v_j) = p_{ij} + q_{ij} \quad \forall i, j \in \{0, 1, ..., n-1\}$$
(8)

such that

$$\beta(v_i) - \beta(v_j) + p_{ij} - q_{ij} = 0 \tag{C1}$$

$$p_{ij} \cdot q_{ij} = 0 \tag{C2}$$

The second non-linear constraint (C2) implies that one of the two integer variables must be 0. To linearize it, we use two binary variables  $a_{ij}, b_{ij}$  and a set of constraints:

$$a_{ij} \le p_{ij} \le a_{ij} \cdot n \tag{C3}$$

$$b_{ij} \le q_{ij} \le b_{ij} \cdot n \tag{C4}$$

$$0 \le a_{ij} + b_{ij} \le 1 \tag{C5}$$

C5 guarantees that the value of both binary variables  $a_{ij}$  and  $b_{ij}$  can not be 1 simultaneously for a given pair i, j. This, in combination with C3-C4, sets one of the two integer variables to 0. We introduce the following constraint to enforce that the offsets assigned to data items are unique:

$$p_{ij} + q_{ij} \ge 1 \tag{C6}$$

It ensures uniqueness because the left hand side of the constraint is the difference of the two memory locations (cf. Eq. 8).

Finally, the linear objective function is:

$$C = \min\left(\sum_{i=0}^{n-1} \sum_{j=i+1}^{n-2} w_{v_i v_j} \cdot (p_{ij} + q_{ij})\right)$$
(9)

The following two constraints are added to ensure that offsets are within range.

$$0 \le \beta_i \le n - 1 \tag{C7}$$

$$\sum_{i=0}^{i=n-1} \beta(v_i) = \frac{n \cdot (n-1)}{2}$$
(C8)

# 4 Approximate data placement

In this section we describe our proposed heuristic and use the insights of our heuristic to extend the heuristic by Chen [13].

#### 4.1 The ShiftsReduce heuristic

ShiftsReduce is a group-based heuristic that effectively exploits the locality of accesses in the access sequence and assigns offsets accordingly. The algorithm starts with the maximum weight vertex in the access graph G = (V, E) and iteratively assigns offsets to the remaining vertices by considering their vertex-to-group weights. Recall from Section 5.2 that the weight of a vertex indicates the count of successive accesses of a vertex with other vertices in S, i.e.,  $w_v =$ 

 $\sum_{u:\{u,v\}\in E} w_{uv}$ . Note that the maximum weight vertex may not necessarily be the vertex with the highest access frequency, considering repeated accesses of the same vertex.

**Definition 2** The vertex-to-group weight  $\alpha(v, g)$  of a vertex  $v \in \mathcal{V}$  is defined as the sum of all edge weights that connect v to other vertices in g, i.e.,  $\alpha(v, g) = \sum_{u \in g: \{u,v\} \in E} w_{uv}$ .

ShiftsReduce maintains two groups referred to as left-group  $g_l$  (highlighted in red in Fig. 7) and right-group  $g_r$  (highlighted in green). Both  $g_l$  and  $g_r$  are lists that store the already computed vertices in V. The heuristic assigns offsets to vertices based on their global and local adjacencies. The global adjacency of a vertex  $v \in V$  is defined as its vertex-to-group weight with the global group, i.e.,  $\alpha(v, g_l \cup g_r)^1$  while the local adjacency is the vertex-to-group weight with either of the sub-groups, i.e.,  $g_l$  or  $g_r$ .

Pseudocode for the ShiftsReduce heuristic is shown in Algorithm 1. The sub-groups  $g_l$  and  $g_r$  initially start at index 0, the only shared index between  $g_l$  and  $g_r$ , and expand in opposite directions as new elements are added to them. We represent this with negative and positive indices respectively as shown in Fig. 7. The algorithm selects the maximum weight vertex  $(v_{\text{max}})$  and places it at index 0 in both sub-groups (cf. lines 3-4).

The algorithm then determines two more nodes and add them to the right (cf. line 6) and left (cf. line 8) groups respectively. These two nodes correspond to the nodes with the highest vertex-to-group weight ( $\alpha$ ), which boils down to the maximum edge weight to  $v_{\text{max}}$ . Lines 10-25 iteratively select the next group element based on its global adjacency (maximum first) and add it to  $g_l$  or  $g_r$  based on its local adjacency. If the local adjacency of a vertex with the left group is greater than that of the right group, it is added to left group (cf. lines 12-14). Otherwise, the vertex is added to the right group (cf. lines 15-17).

The algorithm prudently breaks both inter-group and intra-group tie situations. In an inter-group tie situation (cf. line 18), when the vertex-to-group weight of the selected vertex is equal with both sub-groups, the algorithm compares the edge weight of the selected vertex  $v^*$  with the last vertices of both groups ( $v_p$  in  $g_r$  and  $v_q$  in  $g_l$ ) and favors the maximum edge weight (cf. lines 19-24).

To resolve intra-group ties, we introduce the TIE-BREAK function. The intragroup tie arises when  $v_s$  and  $v_k$  have equal vertex-to-group-weights with g (cf. line 2 in TIE-BREAK). Since the two vertices have equal adjacency with other group elements, they can be placed in any order. We specify their order by comparing their edge weights with the fixed vertex ( $v_n$  for  $g_l$  and  $v_m$  for  $g_r$ ) and prioritize the highest edge weight vertex. The algorithm checks the intragroup tie for every vertex before assigning it to the left-group (cf. line 14) or right-group (cf. line 17).

We demonstrate ShiftsReduce in Fig. 7 for the example in Fig. 6. Vertex a has the highest vertex weight (equal to 4 + 3 + 1 = 8) and is placed at index

<sup>&</sup>lt;sup>1</sup>We abuse notation, using set operations  $(\cup, \setminus)$  on lists for better readability.

Algorithm 1 ShiftsReduce Heuristic

**Input** : Access graph G = (V, E) and a DBC with minimum n empty locations **Output** : Final data placement  $\beta$ 1: $\triangleright v_n =$ fixed element in  $g_l, v_m =$ fixed element in  $g_r$ 2:  $\triangleright v_q = \text{last element in } g_l, v_p = \text{last element in } g_r$ 3:  $\beta \leftarrow \emptyset, v_{\max} \leftarrow \operatorname{argmax}_{v \in V} w_v$ 4:  $g_r$ .append $(v_{\max})$ ,  $g_l$ .append $(v_{\max})$ ,  $V \leftarrow V \setminus \{v_{\max}\}$ 5:  $v^* \leftarrow \operatorname{argmax}_{v \in V} \alpha(v, g_r)$ 6:  $g_r$ .append $(v^*), V \leftarrow V \setminus \{v^*\}, v_p \leftarrow v^*$ 7:  $v^* \leftarrow \operatorname{argmax}_{v \in V} \alpha(v, g_r \setminus \{v^*\})$ 8:  $g_l$ .prepend $(v^*), V \leftarrow V \setminus \{v^*\}, v_a \leftarrow v^*$ 9:  $v_n \leftarrow v_{\max}, v_m \leftarrow v_{\max}$ while V is not empty do 10: $v^* \leftarrow \operatorname{argmax}_{v \in V} \alpha(v, g_r \cup g_l)$ 11: if  $\alpha(v^*, g_l) > \alpha(v^*, g_r)$  then 12: $g_l$ .prepend $(v^*)$ 13: $(v_q, v_n) \leftarrow \text{TIE-BREAK}(v^*, v_q, v_n, g_l)$ 14:else if  $\alpha(v^*, g_l) < \alpha(v^*, g_r)$  then 15: $q_r$ .append $(v^*)$ 16: $(v_p, v_m) \leftarrow \text{TIE-BREAK}(v^*, v_p, v_m, g_r)$ 17:else ▷ inter-group tie 18:if  $w_{v^*v_a} > w_{v^*v_p}$  then 19: $g_l$ .prepend $(v^*)$ 20: $(v_q, v_n) \leftarrow \text{TIE-BREAK}(v^*, v_q, v_n, g_l)$ 21:else 22:  $g_r$ .append $(v^*)$ 23: $(v_p, v_m) \leftarrow \text{TIE-BREAK}(v^*, v_p, v_m, g_r)$ 24: $V \leftarrow V \setminus \{v^*\}$ 25:ASSIGN-OFFSETS( $\beta$ ,  $g_l$ .append( $g_r$ .tail())) 26:

0 in both sub-groups. Vertices c and d have maximum edge weights with a and are added to the right and left groups respectively (cf. lines 6 and 8). At this point, the two sub-groups contain two elements each. The next vertex e is added to  $g_l$  because it has higher local adjacency with  $g_l$  compared to  $g_r$ . In a similar fashion, b and f are added to  $g_r$  and  $g_l$  respectively. ShiftsReduce ensures that vertices at far ends of the two groups have least adjacency (i.e., vertex weights) compared to the vertices that are placed in the middle. Note that the number of elements in  $g_l$  and  $g_r$  may not necessarily be equal. Finally, offsets are assigned to vertices based on their group positions as highlighted in Fig. 7.

Given that we add vertices to two different groups, there are less occurrences of tie compared to algorithms such as Chen's [13] where vertices are always added to the same group. For comparison reasons, we extend Chen's heuristic with tie-breaking in the following section.



Figure 7: Grouping in ShiftsReduce

```
1: function TIE-BREAK(v_s, v_k, v_{\text{fix}}, g)
            if \alpha(v_s, g \setminus \{v_k\}) = \alpha(v_k, g \setminus \{v_k\}) then
 2:
                 if w_{v_s v_{\text{fix}}} > w_{v_k v_{\text{fix}}} then
 3:
 4:
                       v_{\text{fix}} \leftarrow v_s
                       \operatorname{swap}(v_k, v_s)
                                                                                           \triangleright swap positions of v_k, v_s
 5:
                 else
 6:
                        v_{\text{fix}} \leftarrow v_k , v_k \leftarrow v_s
 7:
            else
 8:
                 v_{\text{fix}} \leftarrow v_k, v_k \leftarrow v_s
 9:
             return (v_k, v_{\text{fix}})
     procedure Assign-OFFSETS(\beta, q)
10:
            for i \leftarrow 0 to n - 1 do
11:
                 var \leftarrow variable represented by vertex g_i
12:
                 \beta = \beta \cup \{(var, i)\}
13:
```

#### 4.2 The Chen-TB heuristic

Chen-TB is a heuristic that extends Chen's heuristic with the TIE-BREAK strategy introduced for ShiftsReduce. As shown in Algorithm 2, Chen-TB initially adds three vertices to the group in lines 2-11. In contrast to Chen, we intelligently swap the order of the first two group elements by inspecting their edge weights with the third group element. Subsequently, lines 12-16 iteratively decide the position of the new group elements until V is empty.

The step-wise addition of vertices to the group is demonstrated in Fig. 8. Initially, the algorithm inspects three vertices from V referred to as  $v^0$ ,  $v^1$ , and  $v^2$ . In line 2,  $v^0 = a$  because a has the largest vertex weight ( $w_a = 8$ ). Next,  $v^1 = c$  because c has the maximum edge weight ( $w_{ac} = 4$ ) with a (cf. line 4). Similarly,  $v^2 = d$  because it has the maximum vertex-to-group weight (which is 3) with  $a \cup c$  (cf. line 6). Since the edge weight between a and d (i.e.,  $w_{ad}$ = 3) is higher than the edge weight between c and d (i.e.,  $w_{cd} = 0$ ), we swap the positions of a and c in the group (cf. lines 8-9). At this point, the group elements are c, a, d. The position of a is fixed while d is the last group element. The next selected vertex is e due to its highest vertex-to-group weight with g. In this case, the vertex-to-group weight of d and e is compared with  $c \cup a$  (cf. line 2 in TIE-BREAK). Since d has higher vertex-to-group weight, e becomes the

Algorithm 2 Chen-TB Heuristic

**Input** : Access graph G = (V, E) and a DBC with minimum n empty locations **Output** : Final data placement  $\beta$ 1: $\triangleright v_m$ : fixed element in  $g, v_p$ : last element in g2:  $\beta \leftarrow \emptyset, v^0 \leftarrow \operatorname{argmax}_{v \in V} w_v$ 3:  $g.append(v^0), V \leftarrow V \setminus \{v^0\}$ 4:  $v^1 \leftarrow \operatorname{argmax}_{v \in V} \alpha(v, g)$ 5:  $g.\operatorname{append}(v^1), V \leftarrow V \setminus \{v^1\}$ 6:  $v^2 \leftarrow \operatorname{argmax}_{v \in V} \alpha(v, g)$ 7:  $g.append(v^2), V \leftarrow V \setminus \{v^2\}$ 8: if  $w_{v^0v^2} > w_{v^1v^2}$  then  $v_m \leftarrow v^0$ , swap $(v^0, v^1)$ 9: 10: else  $v_m \leftarrow v^1$ 11:while V is not empty do 12: $v^* \leftarrow \operatorname{argmax}_{v \in V} \alpha(v, g)$ 13: $v_p \leftarrow g.last(), g.append(v^*)$ 14: $(v_p, v_m) \leftarrow \text{Tie-break}(v^*, v_p, v_m, g)$ 15: $V \leftarrow V \setminus \{v^*\}$ 16: 17: ASSIGN-OFFSETS( $\beta$ , g)

last element while the position of d is fixed (cf. line 9 in TIE-BREAK). Following the same argument, the next selected element f becomes the last element while the position of e is fixed. The next selected vertex b and the last element f have equal vertex-to-group-weights i.e. 3 with the fixed elements c, a, d, e. Chen-TB prioritizes f over b because it has the higher edge weight with the last fixed element e.

The final data placements of Chen, Chen-TB and ShiftsReduce are presented in Fig. 9. For the access sequence in Fig. 6, Chen-TB reduces the number of shifts to 23 compared to 27 by Chen, as shown in Fig. 9. ShiftsReduce further diminishes the shift cost to 19. Note that the placement decided by ShiftsReduce is the optimal placement shown in Fig. 3b. We assume 3 or more vertices in the



Figure 8: Chen-TB heuristic. The fixed element is underlined. The green element has higher edge weight with the fixed element and is moved closer to it. ( $t_i$  shows the iteration)

access graph for our heuristics because the number of shifts for two vertices, in either order, remain unchanged.

offsets	0	1	2	3	4	5	shift cos	
Chen	f	b	e	d	c	a	27	
Chen-TB	b	f	e	d	a	c	23	
ShiftsReduce	b	c	a	d	e	f	19	

Figure 9: Final data placements and costs of Chen, Chen-TB and ShiftsReduce. Initial port position marked in green

# 5 Results and discussion

This section provides evaluation and analysis of the proposed solutions on realworld application benchmarks. It presents a detailed qualitative and quantitative comparison with state-of-the-art techniques. Further, it brings a thorough analysis of SOA solutions for RMs.

### 5.1 Experimental setup

We perform all experiments on a Linux Ubuntu (16.04) system with Intel core i7-4790 (3.8 GHz) processor, 32 GB memory, g++v5.4.0 with -O3 optimization level. We implement our ILP model using the python interface of the Gurobi optimizer, with Gurobi 8.0.1 [28].

As benchmark we use OffsetStone [14], which contains more than 3000 realistic sequences obtained from complex real-world applications (control-dominated as well as signal, image and video processing). Each application consists of a set of program variables and one or more access sequences. The number of program variables per sequence varies from 1 to 1336 while the length of the access sequences lies in the range of 0 and 3640. We evaluate and compare the performance of the following algorithms.

- 1. Order of first use (OFU): A trivial placement for comparison purposes in which variables are placed in the order they are used.
- 2. Offset assignment heuristics: For thorough comparison we use Bartley [26], Liao [25], SOA-TB [29], INC [27], INC-TB [14] and the genetic algorithm (GA-SOA) in [30].
- 3. *Chen/Chen-TB:* The RM data placement heuristic presented in [13] and our extended version (cf. Algorithm 2).
- 4. *ShiftsReduce* (cf. Algorithm 1).

- 5. *GA-Ours:* Our modified genetic algorithm for RM data placement described in 5.4.
- 6. ILP (cf. Section 3).

### 5.2 Revisiting SOA algorithms

We, for the first time, reconsider all well-known offset assignment heuristics. The empirical results in Fig. 10 show that the SOA heuristics can reduce the shift cost in RM by 24.4%. On average, (Bartley, Liao, SOA-TB, INC and INC-TB) reduce the number of shifts by (10.9%, 10.9%, 12.2%, 22.9%, 24.4%) compared to OFU respectively. For brevity, we consider only the best performing heuristic i.e., INC-TB for detailed analysis in the following sections.



Figure 10: Comparison of offset assignment heuristics

### 5.3 Analysis of ShiftsReduce

In the following we analyze our ShiftsReduce heuristic.

#### 5.3.1 Results overview

An overview of the results for all heuristics across all benchmarks, normalized to the OFU heuristic, is shown in Fig. 11. As illustrated, ShiftsReduce yields considerably better performance on most benchmarks. It outperforms Chen's heuristic on all benchmarks and INC-TB on 22 out of 28. The results indicate that INC-TB underperforms on benchmarks such as mp3, viterbi, gif2asc,dspstone, and h263. On average, ShiftsReduce curtails the number of shifts by 28.8% which is 4.4% and 6.6% better compared to INC-TB and Chen respectively.

Closer analysis reveals that Chen significantly reduces the shift cost on benchmarks having longer access sequences. This is because it considers the global adjacency of a vertex before offset assignment. On the contrary, INC-TB maximizes the local adjacencies and favors benchmarks that consist only of shorter sequences. ShiftsReduce combines the benefits of both local and global adjacencies, providing superior results. None of the algorithms reduce the number of shifts for *fft*, since in this benchmark each variable is accessed only once. Therefore, any permutation of the variables placement results in identical performance.



Figure 11: Individual benchmark results (sorted in the decreasing order of benefit for ShifsReduce)



#### 5.3.2 Impact of access sequence length

Figure 12: Impact of sequence length on heuristic performance

As mentioned above, the length of the access sequence plays a role in the performance of the different heuristics. To further analyze this effect we partition the sequences from all benchmarks in 6 bins based on their lengths. The concrete bins and the results are shown in Fig. 12, which reports the average number of shifts (smaller is better) relative to OFU.

Several conclusions can be drawn from Fig. 12. First, INC-TB performs better compared to other heuristics on short sequences. For the first bin (0-70), INC-TB reduces the number of shifts by 26.3% compared to OFU which is 10.9%, 7.1% and 2.2% better than Chen, Chen-TB and ShiftsReduce respectively. Second, the longer the sequence, the better is the reduction compared to

OFU. Third, the performance of INC-TB aggravates compared to group-based heuristics as the access sequence length increases. For bin-5 (501-800), INC-TB reduces the shift cost by 25.2% compared to OFU while Chen, Chen-TB and ShiftsReduce reduces it by 38.3%, 38.6% and 41.2% respectively. Beyond 800 (last bin), INC-TB deteriorates performance compared to OFU and even increases the number of shifts by 97.8%. This is due to the fact that INC-TB maximizes memory accesses to consecutive locations (i.e., edge weights) without considering its impact on farther memory accesses (i.e., global adjacency). Fourth, Chen performs better compared to INC-TB on long sequences (average 36.6% for bins 3-6) but falls after it by 6.9% on short sequences (bins 1-2). Fifth, Chen-TB consistently outperforms Chen on all sequence lengths, demonstrating the positive impact of the tie-breaking proposed in this paper. Finally, the proposed ShiftsReduce heuristic consistently outperforms Chen in all 6 bins. This is due to the fact that ShiftsReduce exploit bi-directional group expansion and considers both local and global adjacencies for data placement (cf. Section 4.1). On average, it surpasses (INC-TB, Chen and Chen-TB) by (39.8%, 3.2% and 2.8%) and (0.3%, 7.3% and 4.5%) for long (bins 3-6) and short (bins 1-2) sequences respectively.



Figure 13: Evaluation by benchmark categories

#### 5.3.3 Category-wise benchmarks evaluation

Based on the above analysis, we classify all benchmarks into 3 categories as shown in Table 2. We categorize each access sequence into three ranges i.e., short (0 - 140), long (greater than 140) and very-long (greater than 300). The first benchmark category comprises 19 benchmarks; each containing at least 15% long and 5% very long access sequences. The second and third categories mostly contain short sequences.

Fig. 13 shows that ShiftsReduce provides significant gains on category-I and curtails the number of shifts by 31.9% (maximum up-to 43.9%) compared to OFU. This is 8.1% and 6.4% better compared to INC-TB and Chen respectively. Similarly, Chen-TB outperforms both Chen and INC-TB by 2.3% and 4% respectively. INC-TB does not produce good results because the majority

Category	Benchmarks	Short	Long	Very Long
		Seqs $(\%)$	Sequences $(\%)$	Sequences (%)
	mp3	65.1%	25.6%	9.3%
	veterbi	35.0%	40.0%	25.0%
	gif2asc	17.7%	50.0%	33.3%
	dspstone	63.0%	29.6%	7.4%
	gsm	65.1%	21.6%	13.3%
	cavity	20.0%	40.0%	40.0%
	h263	0.0%	75.0%	25.0%
	codecs	59.7%	33.3%	8.0%
category-I	flex	75.8%	16.9%	7.3%
(ShiftsReduce	sparse	69.6%	22.8%	7.6%
performs better)	klt	54.5%	15.9%	29.6%
	triangle	75.4%	17.2%	7.4%
	f2c	79.5%	15.2%	6.3%
	mpeg2	50.7%	32.4%	16.9%
	bison	63.8%	26.4%	9.8%
	$^{\rm cpp}$	43.7%	33.3%	13.0%
	gzip	50.1%	35.2%	14.7%
	lpsolve	44.6%	38.5%	16.9%
	jpeg	54.5%	15.9%	29.6%
	bdd	85.8%	10.8%	3.4%
category-II	adpcm	93.2%	3.4%	3.4%
(comparable	fft	100.0%	0.0%	0.0%
performance $\pm 2\%$ )	anagram	100.0%	0.0%	0.0%
	eqntott	100.0%	0.0%	0.0%
cotogory III	fuzzy	100%	0.0%	0.0%
(INC performs	hmm	79.7%	10.3%	0.0%
bottor)	8051	80.0%	20.0%	0.0%
Detter)	cc65	84.6%	13.1%	2.3%

Table 2: Distribution of short, long and very long access sequences in Offset-Stone benchmarks

of the benchmarks in category-I are dominated by long and/or very long sequences (cf. Table 2 and Section 5.3.2). Category-II comprises 5 benchmarks, mostly dominated by short sequences. INC-TB provides higher shift reduction (19.6%) compared to Chen (13.2%) and Chen-TB (15.3%). However it exhibits comparable performance with ShiftsReduce (within  $\pm 2\%$  range). On average, ShiftsReduce outperforms INC-TB by 1.1%. INC-TB outperforms ShiftsReduce only on the 4 benchmarks listed in category-III.

### 5.4 GA-SOA vs GA-Ours

Apart from heuristics, *genetic algorithms* (GAs) have also been employed to solve the SOA problem [30]. They start with a random population and compute an efficient solution by imitating natural evolution. However, GAs always take longer computation times compared to heuristics. In order to avoid premature

convergence, GAs are often initialized with suboptimal initial solutions.

This section leverages two genetic algorithms (namely GA-SOA and GA-Ours) for RM data placement. We analyze the impact on the results of GA using our solutions compared to solutions obtained with SOA heuristics as initial population. Both algorithms use the same parameters as presented in [14]. The initial populations of GA-SOA and GA-Ours are composed of (OFU, Liao [25], INC-TB [14]) and (OFU, Chen-TB, ShiftsReduce) respectively.

Experimental results demonstrate that GA-Ours is superior to GA-SOA in all benchmarks. The average reduction in shift cost across all benchmarks (cf. Fig. 15) translate to 35.1% and 38.3% for GA-SOA and GA-Ours respectively.

#### 5.5 ILP results

As expected, the ILP solver could not produce any solution in almost 30% of the instances when given three hours per instance. In the remaining instances, the solver either provides an optimal solution (on shorter sequences) or an intermediate solution. We evaluate ShiftsReduce and GA-Ours on those instances where the ILP solver produces results and show the comparison in Fig. 14. On



Figure 14: Comparison with ILP solution (\* mark benchmarks for which an optimal solution was found)

average, the ShiftsReduce results deviate by 8.2% from the ILP result. GA-Ours bridges this gap and deviate by only 1.3%.

#### 5.6 Summary runtimes and energy analysis

Recall the results overview from Fig. 15. In comparison to OFU, ShiftsReduce and Chen-TB mitigate the number of shifts by 28.8% and 24.5% which is (4.4%, 0.1%) and (6.6%, 2.3%) superior than INC-TB and Chen respectively. Compared to the offset assignment heuristics in Fig. 10, the performance improvement of ShiftsReduce and Chen-TB translate to (17.9%, 17.9%, 16.6%, 5.9%) and (13.6%, 13.6%, 12.3%, 1.6%) for Bartley, Liao, SOA-TB and INC respectively. GA-Ours further reduces the number of shifts in ShiftsReduce by 9.5%. The average runtimes of Chen-TB and ShiftsReduce are 2.99 ms, which is

comparable to other heuristics, i.e., Bartley (0.23 ms), Liao (0.08 ms), SOA-TB (0.11 ms), INC (2.3 s), INC-TB (2.7 s), GA-SOA (4.96 s), GA-Ours (4.98 s) and Chen (2.98 ms).



Figure 15: Results summary

Using the latest RM 4.0 prototype device in our in-house physics lab facility, a current pulse of 1 ns, corresponding to a current density of  $5x10^{11}Amp/m^2$ , is applied to the nano-wire to drive the domains. Employing a 50 nm wide, 4 nm thick wire, the shift current corresponds to 0.1mA. With a 5V applied voltage, the power to drive a single domain translates to 0.5 mW (P = VxI =5Vx0.1mA = 0.5mW). Therefore, the energy to shift a single domain amounts to 0.5pJ (E = Pxt = 0.5mWx1ns = 0.5pJ). The RM 4.0 device characteristics indicate the domains in RM 4.0 shifts at a constant velocity without inertial effects. Therefore, for a 32-bit data item size, the total shift energy amounts to 16pJ without inertia. The overall shift energy saved by a particular solution is calculated as the total number of shifts for all instances across all benchmark multiplied by per data item shift energy (i.e., 16pJ). Using RM 4.0, the shift energy reduction for ShiftsReduce relative to OFU translates to 35%. In contrast to RM 4.0, the domains in earlier RM prototypes show inertial effects when driven by current. Considering the inertial effects in earlier RM prototypes, we expect less energy benefits compared to RM 4.0.

### 6 Related Work

Conceptually, the racetrack memory is a 1-dimensional version of the classical bubble memory technology of the late 1960s. The bubble memory employs a thin film of magnetic material to hold small magnetized areas known as bubbles. This memory is typically organized as 2-dimensional structure of bubbles composed of major and minor loops [31]. The bubble technology could not compete with the Flash RAM due to speed limitations and it vanished entirely by the late 1980s. Various data reorganization techniques have been proposed for the bubble memories [31–33]. These techniques alter the relative position of the data items in memory via dynamic reordering so that the more frequently accessed items are close to the access port. Since these architectural techniques are blind to exact memory reference patterns of the applications, they might excerbate the total energy consumption.

Compared to other memory technologies, RMs have the potential to dominate in all performance metrics, for which they have received considerable attention as of late. RMs have been proposed as replacement for all levels in the memory hierarchy for different application scenarios. Mao and Wang et al. proposed an RM-based GPU register file to combat the high leakage and scalability problems of conventional SRAM-based register files [34, 35]. Xu et al. evaluated RM at lower cache levels and reported an energy reduction of 69% with comparable performance relative to an iso-capacity SRAM [36]. Sun et al. and Venkatesan et al. demonstrated RM at last-level cache and reported significant improvements in area (6.4x), energy (1.4x) and Performance (25%) [20,37]. Park advocates the usage of RM instead of SSD for graph storage which not only expedites graph processing but also reduces energy by up-to 90% [38]. Besides, RMs have been proposed as scratchpad memories [39], content addressable memories [40] and reconfigurable memories [41].

Various architectural techniques have been proposed to hide the RM access latency by pre-shifting the likely accessed DW to the port position [20]. Sun et al. proposed swapping highly accessed DWs with those closer to the access port(s) [37]. Atoofian proposed a predictor-based proactive shifting by exploiting register locality [42]. Likewise, proactive shifting is performed on the data items waiting in the queue [35]. While these architectural approaches reduce the access latency, they may increase the total number of shifts which exacerbates energy consumption.

To abate the total number of shifts, techniques such as data migration [36], data swapping [37], data compression [43], data reorganization for bubble memories [31–33], and efficient data placement [13,39] have been proposed. Amongst all, data placement has shown great promise because it effectively reduces the number of shifts with negligible overheads.

Historically, data placement has been proposed for different memory technologies at different levels in the memory hierarchy. It is demonstrated that efficient data placement improves energy consumption and system performance by exploiting temporal/spatial locality of the memory objects [44]. More recently data placement techniques have been employed in NVM based memory systems in order to improve their performance and lifetimes. For instance [8,45] employ data placement techniques to hide the higher write latency and hence cache blocks migration overhead in an STT-SRAM hybrid cache. Similarly in [9–11], data-placement techniques have been proposed to make efficient utilization of the memory systems equipped with multiple memory technologies. Likewise, data placement in RMs is proposed for GPU register files [46], scratchpad memories [39] and stacks [47] in order to reduce the number of shifts.

In the past, various data placement solutions have been proposed for signal processing in the embedded systems domain (i.e. SOA, cf. 5.2). These solutions include heuristics [14, 25–27, 29], genetic algorithms [30] and ILP based exact

solutions [48–50]. As discussed in Section 5 our heuristic builds on top of this previous work, providing an improved data allocation.

# 7 Conclusions

This paper presented a set of techniques to minimize the number of shifts in RMs by means of efficient data placement. We introduced an ILP model for the data placement problem for an exact solution and heuristic algorithms for efficient solutions. We show that our heuristic computes near-optimal solutions, at least for small problems, in less than 3 ms. We revisited well-known offset assignment heuristics for racetrack memories and experimentally showed that they perform better on short access sequences. In contrast, group-based approaches such as the Chen heuristic exploit global adjacencies and produce better results on longer sequences. Our ShiftsReduce heuristic combines the benefits of local and global adjacencies and outperforms all other heuristics, minimizing the number of shifts by up to 40%. ShiftsReduce employs intelligent tie-breaking, a technique that we use to improve the original Chen heuristic. To further improve the results, we combined ShiftsReduce with a genetic algorithm that improved the results by 9.5%. In future work, we plan to investigate placement decisions together with reordering of accesses from higher abstractions in the compiler, e.g., from a polyhedral model or by exploiting additional semantic information from domain-specific languages.

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