Prof. Dr. AKASH KUMAR

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BIOGRAPHICAL SKETCH

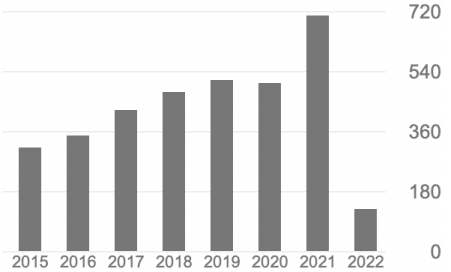
Akash Kumar is a chaired Professor of Processor Design (with tenure) in the department of Computer Science at Technische Universität Dresden (TUD), Germany. From 2009 to 2015, he was with the Department of Electrical and Computer Engineering, National University of Singapore (NUS). He received the joint Ph.D. degree in electrical engineering in embedded systems from Eindhoven University of Technology (TU/e) and National University of Singapore (NUS), in 2009; joint Master's degree from TU/e and NUS in 2005 in embedded systems and Bachelor of Computer Engineering degree from NUS in 2002.

His research interests span various aspects of design automation in the context of embedded real-time systems with particular emphasis on reliable, resource-efficient and predictable architectures for embedded systems, including FPGA-based architectures. His research spans across various layers in the system design from hardware design to application analysis. He has published close to 210 articles in premier international conferences and journals in the area of design automation, including 3 monographs and 3 book chapters. Together with his research group, he has released many **open-source tool flows** for system design and analysis to allow the community to reproduce their results and to further research in the related areas.

He serves (or has recently served) on the program committee of renowned conferences in the area like DAC, DATE, FPL and CASES. He was the program chair of International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES'18 and '19), Embedded Systems for Real-Time Multimedia (ESTIMedia '17), subcommittee chair for several editions of Design Automation and Test in Europe (DATE) conference and Brief Presentations Chair for Real-time Systems Symposium (RTSS'19) and Associate Editor for Elsevier Microprocessors and Microsystems journal for 2013-2017 and ACM Transactions on Embedded Computing Systems (TECS) special issue. He is currently an associate editor for IEEE Transactions on Circuits and Systems II, IEEE Embedded Systems Letters (ESL), IEEE Design and Test and MDPI Electronics. He was the program chair for IEEE International Conference on Field Programmable Logic and Applications 2021.

His work has received Best Paper Award at DATA 2018, and best paper award nominations at DATE 2015, 2017 and 2020, FPL 2014, GLSVLSI 2014, ISVLSI 2020 and Supercomputing Conference 2015. His group also received HiPEAC Technology transfer award 2019. His current publication and citation profile according to Google scholar can be found at https://scholar.google.com/citations?hl=en&user=7Q6OSvsAAAAJ. His current H-index is 35, with a growing citation profile as evident from the graph below. According to CS-rankings, he is the second most published Professor in top conferences at TU Dresden in Computer Science (http://csrankings.org/#/fromyear/2011/toyear/2021/index?all&europe). The DBLP profile can be found at https://dblp.uni-trier.de/pers/hd/k/Kumar_0001:Akash.

	All	Since 2017
Citations	4284	2760
h-index	35	28
i10-index	98	76



43 ▼ TU Dresden	1.9	15
Faculty	*# Pubs*	*Adj. #*
Bjoern Andres VISION	26	5.5
Akash Kumar 0001 EDA	19	4.8
Raimund Dachselt HCI	19	6.3
Wolfgang Lehner DB	16	3.3
Sebastian Rudolph AI	14	5.4
Christel Baier LOGIC	11	2.6
Stefan Gumhold VISION	10	2.1
Hermann Härtig EMBEDDED	8	2.3
Christof Fetzer	5	0.9

RESEARCH INTERESTS

Design automation of embedded systems, reliability optimization, fault-tolerant and predictable architecture design, approximate computing, electronic design automation for FPGAs and emerging technology, partially reconfigurable architectures.

EDUCATION

May 2005 – Apr 2009 Eindhoven University of Technology (TUe) & National University of Singapore

- **PhD** thesis title: *Analysis, Management and Design of Multimedia Multiprocessor Systems***.**
- Published over 20 papers in leading system design automation conferences/ journals.
- Worked in close collaboration with many companies: **Silicon Hive (Intel), NXP Semiconductors, Philips**.
- Attended HiPEAC summer school on **Advanced Comp. Arch. and Compilation for Embedded Systems** in 2006.
- Attended ASCI spring school on **Embedded Systems** in 2006.

Jan 2003 – Dec 2004 National University of Singapore & Eindhoven University of Technology (TUe)

- **Master** of Technological Design (Embedded Systems). **GPA: 4.70/5.00.**
- Master's thesis title: *High-Throughput Reed Solomon Decoder for Ultra Wide Band.*
- Received **Certificate of Merit** for the research done during internship at Philips Research Labs.

Jul 1999 – Dec 2002 National University of Singapore (NUS)

- Accelerated **B. Eng**. (Computer Engineering) Program, **First Class Honours, GPA: 4.75/5.00.**
- Class **Valedictorian** (chosen out of about 800 students) and **Dean's List** on **4** occasions.

WORK EXPERIENCE

Oct 2015 – contd. Chair Professor of Processor Design – Technische Universität Dresden (TUD), Germany

- Pursuing research in the framework of CFAED (Center For Advancing Electronics Dresden)
- Supervising students from undergraduate to post-graduate for research
- Erasmus co-ordinator for Computer Science since 2017
- **Dean of Studies since 2022**

Jul 2009 – Sep 2015 Assistant Professor – National University of Singapore (NUS), Singapore

- Joined NUS in Jul 2009 as a Visiting Fellow. Worked as an Assistant Professor from Jun 2011.
- Teaching courses offered by the Electrical and Computer Engineering (ECE) department.
- Pursuing research in the area of embedded multi-processor systems.
- Supervising students from undergraduate to post-graduate for research.

Sep 2013 – Sept 2015 Guest Professor – Beijing University of Technology (BJUT), Beijing, China

- Give invited lectures at BJUT on real-time embedded systems.

Jul 2011 – Sept 2015 Xilinx Trainer – Active Media Singapore

- Provide training on Xilinx FPGA architecture and design methodology.
- Authorized to train on Zynq, Embedded Systems, Advanced features and techniques of Embedded Systems development, FPGA design, Advanced FPGA design, designing for performance, etc. courses.

May 2005 – Jun 2009 Research Assistant – Eindhoven University of Technology (TUe), The Netherlands

- Conduct research on embedded multiprocessor systems in order to make them predictable.
- Education: design and evaluate lab exercises for under-graduate and post-graduate courses.

Jan 2004 – Dec 2004 Research Intern – Philips Research Laboratories, The Netherlands

- Developed a high throughput, ultra-low power Reed-Solomon decoder for Ultra Wide Band.
- **2 International Patents** filed over the work done during this stay, and **3 international publications**.

Jan 1999 – Dec 2003 Boarding Tutor, Raffles Institution Boarding School, Singapore

- Manage, supervise, motivate and teach a block of 90 students.
- Handle contingencies and organize activities for personality development of boarders.

Jun 2002 – Dec 2002 Intern – Merrill Lynch, Singapore

- Developed various automated applications using Java and Visual Basic for Applications.
- Conduct trainings for ML employees in database management system.

Jun 2001 – Aug 2001 Research Fellowship, California Institute of Technology, US

- 1 of the **3 students selected** from the entire National University of Singapore for this fellowship.
- Developed and implemented a scan-matching algorithm for sensor-based motion planning.

PATENTS

- **Method and Apparatus for Syndrome Calculation**
  International Application Number: PCT/IB2006/052151, filed on June 28, 2006.
  Europe Patent Application Number: 05105878.2, filed on June 30, 2005.
- **Pipelined Reed-Solomon Decoder**
  International Application Number: PCT/IB2006/054745, filed on Dec 11, 2006.
  Europe Patent Application Number: 05111971.7, filed on Dec 12, 2005.

HONOURS AND AWARDS

- Google Scholar Citations $\geq$ 4,100; H-index 34 (Dec 2021).
- Best paper award at International Conference on Data Science, Technology and Applications (DATA) 2018.
- Best presentation award at Software and Compilers for Embedded Systems (SCOPES) 2016.
- Best paper candidate in the following conferences
  a. IEEE International Symposium on VLSI (ISVLSI) 2020.
  b. Design, Automation & Test in Europe (DATE) 2015, 2017, 2020.
  c. High Performance Computing, Networking, Storage and Analysis (SC) 2015.
  d. Field Programmable Logic and Applications (FPL) 2014.
  e. Great Lakes Symposium in VLSI (GLSVLSI) 2014.
- Received **HiPEAC Technology Transfer Award** in 2019.
- Received **Annual Teaching Excellence Award** in 2015 at NUS, Singapore – awarded the TOP rating for teaching in the entire department with close to 100 faculty members.
- Placed on **Honour Roll of teachers** in 2014 – top 5% of faculty with total strength of 300.
- **Singapore Mathematical Olympiad Gold** medallist.
- **1st place** in **IEEE – NTU Mathematics Olympiad**.
- Awarded **National Talent Search Scholarship** by **Human Resource Development Ministry, India.**
- Recipient of **SIA Scholarship** for Pre-University and Bachelors study in **RJC** and **NUS**.
- Awarded **DTI scholarship** (managed by EDB) for **Masters in Embedded Systems** in NUS.
- **Runner-up** in the first International **IEEE Extreme** Online Programming contest.
- **On-stage finalists** in first International **Tata Crucible** in NUS – "India's toughest **business** Quiz".
- **10th place** in annual **ACM** International Collegiate Programming Contest regional contest (ICPC).

RESEARCH AND TEACHING GRANTS

- X-ReAp: Cross(X)-Layer Runtime Reconfigurable Approximate Architecture, DFG (German Research Foundation).
  Principal Investigator, Euro 329,600, 1/2022-12/2024.
- CirroStrato: Novel reconfigurable transistors for IP protection of electronic components
  BMBF ZEUS Call
  Principal Investigator, Euro 515,746, 03/2021-02/2024.
- Extreme Energy-efficient Edge Cloud Hardware
  BMBF Green ICT Call.
  Co-Principal Investigator, Euro 34.300, 10/2020-06/2021. Total Project Value, Euro 250.000.
- SARA: Safety-Aware Relocation of functions in a multi-core computer Architecture
  Software Campus (BMBF).
  Principal Investigator, Euro 99.980, 03/2021-02/2023.
- COMPOSES: Accelerated OpenCV Image Processing for Embedded Systems
  Software Campus (BMBF).
  Principal Investigator, Euro 49.900, 11/2020-10/2021.
- Reliable Batteryless Networks: Making Computer Systems More Sustainable and Efficient
  Prediction Framework, cfaed open postdoc Call (DFG).
  Co-Principal Investigator, Euro 145.000, 10/2020-08/2022.
- Design Space Evaluation Framework for Future Circuit Technologies
  cfaed open postdoc Call (DFG).
  Principal Investigator, Euro 145.000, 09/2020-08/2022.
- SecuREFET: Secure circuits through inherent reconfigurable FET.
  DFG Special Priority Program.
  Principal Investigator, Euro 298.200, 07/2020-06/2023, Total Project Value, Euro ~700,000 in collaboration with NaMLab Dresden.
- ReLearning: self-learning and flexible electronics through inherent transistor reconfiguration (ESF/SAB)
  Co-Principal Investigator, Euro 152,112, 03/2020-02/2022.
- HANS: Hardware Accelerated Neural Network as a Service, Software Campus (BMBF).
  Principal Investigator, Euro 49.997, 03/2020-06/2021.
- PRÄKLIMA Fassade, AiF Projekt GmbH.
  Principal Investigator, Euro 189.000, 08/2019-06/2022, Total Project Value, Euro ~950,000 shared among 3 companies and two institutes at TU Dresden.
- LabVIEW-on-Chip Project, National Instruments.
  Co-Investigator, Euro 300,000, 04/2019-03/2022. Total Project Value, Euro ~900,000 shared equally among 3 PIs.
- ReAp: Runtime reconfigurable approximate architecture, DFG (German Research Foundation).
  Principal Investigator, Euro 191,600, 2/2018-1/2021.
- Emulation platform for wildly heterogeneous chips, Orchestration Seed Grant in cfaed (DFG).
  Principal Investigator, Euro 50,000, 1/2017-12/2017.
- FPGA Floorplanner for partially reconfigurable systems, Huawei Project.
  Principal Investigator, Euro 103,500, 11/2016-10/2017.

- Enabling very large-scale integration for novel materials, Orchestration Seed Grant in cfaed (DFG).
  Principal Investigator, Euro 50,000, 1/2016-12/2016.
- Thermal Aware 3-Dimensional Multi-Core Systems Design, MoE Tier 2 Grant.
  Principal Investigator, S$571,000, 11/2014-10/2017.
- Development of Low-Cost Low-Power FPGA-Based Brain Computer Interface System, MoE Tier 1 Grant
  Principal Investigator, S$179,990, 03/2014-02/2017.
- Fault-tolerant Multi-processor Systems, DSO National Laboratories
  Principal Investigator, S$429,600, 06/2012-05/2015.
- Partially Reconfigurable Heterogeneous Multiprocessor System-on-Chip, MoE Tier 1 Grant
  Principal Investigator, S$179,990, 08/2011-07/2014.
- A Power-Efficient Heterogeneous Architecture and Run-Time Manager for Data Center Servers, A*Star Grant
  Co-Investigator, S$496,555, 08/2011-04/2013.
- Secured Large Scale Shared Storage System, A*Star Grant
  Co-Investigator, S$ 1,815,515, 08/2011-07/2014.
- Integrated Classroom Learning App for Adaptive Learning and Response Analytics, NUS Provost's Office
  Principal Investigator, S$40,000, 01/2014-12/2015.
- Web-based toolkit for enhanced learning experience in digital fundamentals courses, NUS CDTL
  Principal Investigator, S$19,200, 08/2010-07/2012.
- Investigating feasibility of using fast reconfigurable logic in a typical MPSoC platform
  Principal Investigator, € 5,000, 01/2007-04/2007.
- A run-time admission controller for multiple applications on FPGA
  Principal Investigator, € 5,000, 09/2007-12/2007.

TEACHING

Following are the courses that I have (co-)taught during my appointment at TUe, NUS and TUD. I have had an opportunity to teach classes of varying sizes – from 400 students to only 12 students in a class. In all my courses I ensure that students need to work on design problems in small groups to understand the concepts better. **The first two course are conducted in both German and English language.**

- Computer Architecture
- Introduction to Computer Engineering
- Reconfigurable Computing
- Embedded Hardware Systems Design
- Real-Time Embedded Systems
- Digital Design Fundamentals
- Implementing Large Scale Embedded Processors on Deep-Submicron Silicon

GRADUATE STUDENTS SUPERVISION

Post-Doctoral Researchers

Current

- *Steffen Maercker (PhD: Technical University of Dresden)*
- *Salim Ullah (PhD: Technical University of Dresden)*

Past

- Mark Wijtvliet (PhD: Eindhoven University of Technology)
- Siva Satyendra Sahoo (PhD: National University of Singapore)
- Tuan Duy Anh Nguyen (PhD: National University of Singapore)
- Golsa Moayeri Pour (PhD: Purdue University)
- Semeen Rehman (PhD: Karlsruhe Institute of Technology)
- Seetal Potluri (PhD: Indian Institute of Technology Madras)
- Mohammad Shihabal Haque (PhD: University of New South Wales, Australia)
- Liang Tang (PhD: University of New South Wales, Australia)
- Rui Santos (PhD: University of Porto, Portugal)
- Amit Kumar Singh (PhD: Nanyang Technological University)

Current PhD Students

- Siddharth Gupta (2021-): Dealing with adversarial attacks in Deep Neural Networks
- Armin Darjani (2021-): Designing secure hardware using emerging nano-technology
- Nima Kavand (2021-): Securing the EDA for RFET-CMOS co-design
- Max Sponner (2021-): Research and Development of Partially Reconfigurable Embedded Deep Learning Inference Accelerator, ***in collaboration with Infineon.***
- Elias Trommer (2020-): Ultra Low Power Neural Processing Architectures, ***in collaboration with Infineon.***
- Paul Jungmann (2020-): using machine learning to predict device lithography parameters, ***in collaboration with GlobalFoundries.***
- Cecilia De la Parra (2018-): digital hardware for approximate computing of deep neural networks, ***in collaboration with Robert Bosch.***
- Zahra Ebrahimi (2018-): Designing reconfigurable approximate arithmetic operators
- Behnaz Ranjbar (2018-): Thermal-aware design of mixed-criticality systems
- Shubham Rai (2016-): Design automation for emerging technologies
- Martin Brüstel (2016-): Approximate computing for reducing power and area requirements
- Michael Raitza (2015-): Novel circuits using silicon nano-wire transistors

PhD Students Graduated/Submitted Thesis

- Salim Ullah (2016-2021): Design, Analysis, and Applications of Approximate Arithmetic Modules
- Nusrat Jahan Lisa (2017-2020): Heterogeneous system design for data base acceleration using FPGAs
- Mark Wijtvliet (2014-2020): Blocks, a reconfigurable architecture combining energy efficiency and flexibility
    - PostDoc Researcher at TU Dresden
- Siva Satyendra Sahoo (2014-2018): Designing for Cross-layer Reliability.
    - Senior Staff Enginer at SAIT, Samsung, India
- Nguyen Duy Anh Tuan (2013-2017): Partially Reconfigurable Heterogeneous Multi-Processor Systems On-Chip
    - Staff Research Engineer, Xilinx, Singapore
- Pham Nam Khanh (2012-2016): Multi-Objective Design Automation For Reconfigurable Multi-Processor Systems
    - Lead Data Scientist at INSPECTORIO, Vietnam
- Li Ang (2012-2016): GPU Performance Modelling And Optimization
    - Staff Scientist at Pacific Northwest National Laboratory, USA
- Hoo Chin Hau (2012-2017): Parallel Routing For Field Programmable Gate Arrays
    - Geospatial machine learning researcher at Grab, Singapore
- Anup Kumar Das (2011-2014): Design methodologies for reliable and energy-efficient multiprocessor systems
    - Assistant professor at Drexel University, USA

- Amit Kumar Singh (2009-2012): Run-time mapping of communicating tasks on multi-processor platforms.
    - Assistant professor at University of Essex, UK
- Ahsan Shabbir (2007-2011): Resource mapping and management for predictable multi-processor platforms.

TECHNICAL PROGRAM COMMITTEES

I have participated in many technical program committees. Most of them are leading conferences in the area, like DAC, DATE, ASPDAC, CASES and FPL. A (partial) list of recent engagements is provided below.

- ASPDAC (Asia and South Pacific Design Automation Conference): 2015-2020
- CASES (Compilers, Architecture and Synthesis for Embedded Systems): 2015-2021
    - Program Co-chair: 2018
    - Program Chair: 2019
- DAC (Design Automation Conference): 2015, 2016, 2020, 2021, 2022
    - Topic co-chair: 2022
- DATE (Design Automation and Test in Europe): 2015-2019
    - Topic co-chair: 2017
    - Topic chair: 2018, 2019
- DSD (Digital Systems Design): 2015-2018
- Estimedia (Embedded Systems for Real-Time Multimedia): 2016, 2017
    - Program co-chair: 2017
- ESWEEK (Embedded Systems Week: 2021, 2022
    - Education co-chair: 2021
    - Education chair: 2022
- FPL (Field Programmable Logic and Applications): 2015-2021
    - Program Chair: 2021
- GLSVLSI (Great Lakes Symposium on VLSI): 2015-2021
- MOMAC (Multi-Objective Many-Core Design): 2016
- RAW (Reconfigurable Architecture Workshop): 2016
- RTSS-BP (Real Time Systems Symposium – Brief Presentations): 2019
    - Program Chair: 2019
- SCOPES (Software and Compilers for Embedded Systems): 2015- 2021
- SocPros (Soft Computing for Problem Solving): 2020
- VLSID (VLSI Design and Embedded Conference): 2015, 2016, 2020
    - Topic chair: 2020

JOURNAL EDITORSHIPS AND REVIEW

- I served as an associate editor for Elsevier Microprocessors and Microsystems: Embedded Hardware Design (MICPRO), a guest editor for ACM Transactions on Embedded Computing Systems (TECS) and ACM Transactions on Reconfigurable Technology Systems (TRETS). I am currently serving as an associate editor for IEEE Design and Test, IEEE Transactions on Circuits and Systems II, IEEE Embedded Systems Letters and MDPI Electronics. In addition to editorships, I have also reviewed many journal papers for the following journals in the last five years.
- Associate Editor IEEE Design and Test (DnT): 2022-
- Associate Editor IEEE Transactions on Circuits and Systems II (TCAS-II): 2022-
- Associate Editor IEEE Embedded Systems Letters (ESL): 2020-

- Associate Editor MDPI Electronics: 2020-
- Associate Editor Elsevier Microprocessors and Microsystems: Embedded Hardware Design: 2015-2018
- IEEE Design and Test (DnT)
- IEEE Transactions on Computers (TC)
- IEEE Transactions on Computer Aided Design (TCAD)
- IEEE Transactions on Emerging Topics in Computing (TETC)
- ACM Transactions on Architecture and Compiler Optimization (TACO)
- ACM Transactions on Embedded Computing Systems (TECS)
- ACM Transactions on Design Automation of Electronics Systems (ToDAES)
- ACM Transactions on Reconfigurable Technology Systems (TRETS)
- Elsevier Journal of Systems Architecture (JSA)
- Elsevier Microprocessors and Microsystems: Embedded Hardware Design (MICPRO)
- Elsevier Simulation Modeling Practice and Theory (SIMPAT)
- Elsevier Journal of Microelectronics Reliability (JMR)
- Elsevier Journal of Parallel and Distributed Computing (JPDC)

OTHER ACTIVITIES

- **Gliding** for 4 years in Eindhoven University student flying club. Certified **solo glider pilot**.
- Committee member of **Indian Instrumental Ensemble (IIE)** at NUS and a senior **violin** player. Organised and participated in annual concerts on and off-campus.
- Learnt **North-Indian classical music** (Hindustani) for over 8 years; performed on many occasions.
- Learnt and performed various **Latin and Style-dances** since last 8 years.
- Play **badminton** and **squash** regularly.

LANGUAGE SKILLS

- **English, Dutch, German & Hindi:** Fluent in reading, writing and conversing.

LIST OF REFEREES

- **Prof. Dr. Henk Corporaal:** PhD advisor at TU Eindhoven (2005-2009) and Masters Project.
  Email: h.corporaal@tue.nl. Tel: +31-40-247-5462/5195.
- **Prof. Nikil Dutt:** Research collaborator, Chancellor's Professor at UC Irvine.
  Email: dutt@uci.edu. Tel: +1-949-824-7219.
- **Prof. Samarjit Chakraborty:** Research collaborator, William R. Kenan, Jr. Distinguished Professor, University of North Carolina, Chapel Hill.
  Email: samarjit@cs.unc.edu. Tel: +1- 919-590-6038.
- **Prof. Dr. Sergei Sawitzki:** Supervisor at Philips Research. Currently at Univ. of App. Sciences, Wedel, Germany.
  Email: saw@fh-wedel.de. Tel: +49-4103-8048-37.
- **Prof. Dr. Yajun Ha:** PhD advisor and colleague at National University of Singapore (2005-2014). Currently at ShanghaiTech University.
  Email**:** hayj@shanghaitech.edu.cn. Tel: +86-021-20685371.