Leakage and Performance Aware Resource Management for 2D Dynamically Reconfigurable FPGA Architectures

Siqi Wang, Nam Khanh Pham, Amit Kumar Singh, Akash Kumar
Department of Electrical and Computer Engineering, National University of Singapore, Singapore
{a0077818, phamnamkhanh, amit.singh, akash}@nus.edu.sg

Abstract—The variety of applications for field programmable gate arrays (FPGAs) is continuously growing, thus it is important to address power consumption issues during the operation. As technological node shrinks, leakage power becomes increasingly critical in overall power consumption of FPGA. The technique of configuration pre-fetching (loads configurations as soon as possible) adopted to achieve high performance is one of the major reasons of leakage waste since regions containing reconfiguration information cannot be powered down in between the time gap of reconfiguration and execution. In this work, we present a heuristic approach to minimize the leakage power consumption for two-dimensional reconfigurable FPGA architectures. The heuristic scheduler is based on list scheduling and exploits dynamic priority for selecting the tasks into schedule order and a cost function for cell allocation. Farthest placement scheme is adopted for anti-fragmentation purpose. The cost function provides control to minimize the leakage dissipation and schedule length.

I. INTRODUCTION

Field programmable gate arrays (FPGAs) are increasingly used in current technologies. They are popular choices for digital circuits implementation because of their short design cycle, fast speed, and low cost compared to the traditional application specific integrated circuit (ASIC). The run time partial reconfigurable FPGA architecture provides even greater flexibility. Extensive studies have been done for performance improvements of FPGAs. Task execution time and power consumption are popularly discussed topics [1], [2].

The leakage power of transistor does not contribute functionally in the operation of FPGA. It is primarily the result of unwanted sub-threshold current in transistor channel. As technology advances to shrink the feature size, leakage power becomes more and more critical in the overall power consumption of FPGAs. In the recent generation of 65nm, 40nm, and 28nm FPGAs, leakage power consumption constitutes around 50% of the overall power consumption [3]. The introduction of high-threshold voltage sleep transistors enables FPGA to be powered gated when not in use to manage active leakage power [4]. The technique that divides FPGA into smaller portions and uses sleep transistors to power gate the region has reduced the leakage power consumption significantly [5].

In addition, for run-time reconfigurable FPGAs, configuration pre-fetching is a well-established approach to hide the reconfiguration time in order to reduce the overall execution time. However, due to the involved task dependencies, tasks can only execute after its predecessors have finished executions. This often introduces a time gap between end of configuration and start of execution, as shown in Figure 1, which results in significant leakage waste. The region containing configuration bits cannot be powered gated during this time gap since it needs to preserve the configuration. Therefore, reducing leakage waste in such scenarios is critical and highly desired.

The ability to reconfigure and power-gate (turn-off) part of the FPGA devices brings two types of architecture: one dimensional reconfigurable and two dimensional reconfigurable architectures, as shown in Figure 2. The shaded area represents the task placement on FPGA. For 1D architecture, the configurable logic blocks (CLBs) are partitioned in forms of columns. Tasks are placed on predefined columns and span the whole column. One column is therefore called one Reconfigurable Unit (RU). The sleep transistors gate the power of the predefined column (RU) to power off when not in use. Recent technologies enable architectures with dynamically controlled power gating capabilities, by which logic clusters can be selectively powered-down at run time [6]. Task placements are therefore not constrained in one dimension. Such architectures allow RUs to be of any combinations of CLBs and are called 2D reconfigurable architectures. Two-dimensional architecture is more flexible and can save more space and energy when compared to column-by-column one-dimensional reconfigurable architectures. The minimizations of the leakage waste are studied at different levels. In this work, we focus on the system level solution. In order to reduce the leakage power consumption, we optimize the schedule such that the reconfiguration is placed as close as possible to the execution in time in order to minimize the standby period of the RUs.

We propose list based heuristic scheduling for 2D architectures (LBHS2D) to address the leakage minimization problem for 2D architectures. The LBHS2D adopts list scheduling skeleton. It implements dynamic priority scheme for task sorting, and cost function with farthest placement scheme for task placement.

The rest of the paper is organized as follows: Related works are reviewed and discussed in Section II, followed by the problem definition in section III. The proposed LBHS2D approach is discussed in Section IV. Experiments and results are discussed in Section V, and a conclusion in Section VI.

II. RELATED WORKS

The scheduling problem on 1D reconfigurable architectures is proven to be an NP-complete problem. Therefore, most of the research works aim at developing heuristic approaches. In [7], an efficient technique to schedule real-life applications on
FPGA is proposed, but partial reconfiguration and resource constraint has not been considered. In [2], the authors proposed a two stage approach, in which a schedule is first generated by a performance driven task scheduler, and then refined to reduce the leakage power without compromising the performance. Hsieh et al. [8] proposed an enhanced leakage-aware scheduling algorithm (ELAA) that comprises of three stages of binding the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline. Another work proposed in [9] considers a three stage leakage aware placer which splits the reconfiguration and execution of the task together, assigning each task block a priority, and finally placing with a split aware placer which splits the reconfiguration and execution only when the schedule cannot meet the deadline.
Algorithm 1: LBHS2D Algorithm

Input: Task graph \( S, p \)
Output: Leakage aware schedule
1. Put source tasks (tasks with no predecessors) \( \{ t_i \in S : parent(t_i) = 0 \} \) into set \( readyNodeList \);
2. while \( readyNodeList \neq \emptyset \) do
3. Calculate priority of tasks in \( readyNodeList \) (by Equation 1);
4. Choose the task \( t \) with maximum priority;
5. Choose the best cell \((c, r)\) for task \( t\) (by Algorithm 2);
6. if \( \text{Child tasks of } t \text{ are not already added to } \) \( readyNodeList \) then
7. Add the child tasks to \( readyNodeList \);
8. end
9. Remove task \( t \) from \( readyNodeList \);
10. Add task \( t \) to \( scheduledNodeList \);
11. end

longest path in the task graph from this task to the exit task;
LK: leakage waste caused by scheduling the task;
C: number of columns required by the task;
R: number of rows required by the task;
EEST: earliest execution start time of the task;
ERST: earliest reconfiguration start time of the task;
RT: the reconfiguration time of the task, which is proportional to \( C \times R \);
The metrics to be considered in deciding which task to be scheduled next are the overall execution time and the leakage power consumption. Therefore here we include the following:
- Bottom level (BL): to schedule the tasks with more descendants first.
- Leakage power (LK): not to schedule the tasks those have more leakage power in current FPGA condition.
- Earliest execution time (EEST): to schedule the tasks that can start early first.
\( \alpha, \beta, \gamma \) are the coefficient that are adjustable for better schedule results for different parallelism of task graphs.

B. Farthest Placement Placer

The algorithm to find the best RUs for a task is presented in Algorithm 2. To find the best cell, the placer checks all the RUs and choose the cell \((c, r)\) proving least cost \( K \), which is computed as follows:

\[
K = \alpha \times \text{LK} + (1 - \alpha) \times \text{EEST} \tag{3}
\]

where \( \text{LK} \) represents leakage power, \( \text{EEST} \) represents the earliest execution starting time for the task to be placed on the block of cells. \( \alpha \) is a coefficient to compromise between amount of leakage power and scheduled length which can be set to any value between 0 and 1. Large value of \( \alpha \) will result in more concentration of leakage power minimization in the scheduling, while a small value of \( \alpha \) will concentrate more on the scheduled length optimization. This parameter gives designer flexibility to compromise between leakage power dissipation and scheduled length.

The algorithm checks all the blocks of the task size and find the block with the least cost \( K \). If more blocks are available with the same least cost, the algorithm chooses the block that is nearer to the boundary of the FPGA. This farthest placement criterion is the anti-fragmentation technique used to facilitate better future placements such as easier fitting of larger tasks into the middle part of FPGA.

Algorithm 2: Best Placement Cell Search Algorithm

Input: FPGA, task \( t \)
Output: Best placement cell \((c, r)\)
1. for each cell: \( c, r \in R \) do
2. Put task \( t \) on the block begin with \((c, r)\);
3. Calculate the cost \( \text{cost}_{\text{new}} \) for task \( t \) on the block;
4. if \( \text{cost}_{\text{new}} > \text{cost}_{\text{min}} \) then
5. Update minimum cost value \( \text{cost}_{\text{min}} \);
6. Update best placement cell \((c, r)\);
7. end
8. if \( \text{cost}_{\text{new}} = \text{cost}_{\text{min}} \) then
9. Check the distance of the cells \((c, r)\) to the boundary of FPGA;
10. if new cell \((c, r)\) is nearer to the boundary than old cell then
11. Update best placement cell \((c, r)\);
12. end
13. end
14. end

V. EXPERIMENTS AND RESULTS

A series of task graphs are generated and scheduled by our proposed approaches in order to evaluate the quality of obtained results. The approaches are compared with existing performance driven scheduler (PDA) proposed in [1], Enhanced Leakage Aware Algorithm (ELAA) proposed in [8], and the Napoleon (NAP) heuristic proposed in [11]. The experiments are designed to test the performance of the scheduler; therefore no hard deadline is specified in the experimental settings.

PDA [1] algorithm considers only the scheduled length, while ELAA [8] makes sure the minimum leakage dissipation when meeting the deadline constraints. Since no deadlines are specified in the context, ELAA will always return zero leakage dissipation. The parameter \( \alpha \) in Equation 3 is set to different values in the experiments to explore the trade-offs between scheduled length and leakage power dissipation. NAP algorithm proposed in [11] exploits limited de-configuration method which introduces large amount of leakage dissipation. Therefore the implementation of the algorithm omits the limited de-configuration scheme for fair comparison.

The algorithms are implemented in Java language, and the experiments are performed on an Intel Core i5 2.30 GHz CPU with 4GB RAM. A series of synthetic task graphs are generated by the TGFF tool [12]. 5 sets of task graphs with 10 task graphs in each set are generated. The number of tasks in a task graph in each set is 10, 20, 30, 40 and 50. The tasks have \( l_t \) in range of \( 15 \pm 10 \) time units, \( c_t \) in range of \( 4 \pm 3 \) cells and \( r_t \) in range of \( 3 \pm 2 \) cells. In order to see the effectiveness of approaches to real-life applications, task graphs of JPEG encoder [1], MPEG4 decoder [13] and MP3 decoder [14] are also considered with their specifications provided in respective references.

The comparison of different approaches are mainly based on the overall scheduled length and the leakage power dissipation. The scheduled length is measured in time units, and the leakage dissipation is measured in energy units. One energy unit is defined as the leakage power dissipation of 1 cell (RU) during 1 time unit. The leakage power of the task is calculated as defined in equation 2. The overall leakage power of a task graph is the sum of all individual tasks. The leakage power of the task set is the average of all the task graphs in the set.
A. Schedule Length and Leakage Dissipation

Figure 3 (a) shows schedule length for application sets for an FPGA having 10 row and 10 columns of RUs. It can be observed that as the number of tasks in the task graph increases, the overall schedule length increases. Further, LBHS2D provides scheduled length in between best performance scheduler (PDA) and best leakage scheduler (ELAA). Figure 3 (b) shows corresponding leakage results. It can be observed that LBHS2D reduces the leakage waste significantly compared to PDA. On an average, LBHS2D reduces leakage waste by 33.72% when compared to PDA.

B. Leakage Dissipation and Scheduled Length Trade-offs

The parameter a in Equation 3 gives the designers flexibility to control over the scheduled length and leakage power dissipation. Figure 4 shows the results of LBHS2D for different values of a, and existing approaches PDA and ELAA. The results shown are for task graphs of 30 tasks on an FPGA of size 10 × 10. The figure shows the experimental Pareto-front, which indicates that designers can choose different values of a to achieve different objectives. Additionally, it can be observed that when parameter a approaches 0.9, the LBHS2D algorithm can achieve zero leakage power dissipation with scheduled length shorter than ELAA. Similar behavior has been observed for other application sets.

C. Real-life Applications Case Study

Table I shows schedule length and leakage dissipation results for real-life applications JPEG encoder, MPEG4 decoder and MP3 decoder when different approaches are employed. The shown results are for an FPGA size of 6 × 6. The parameter a is set to 0.5 in our LBHS2D approach. It can be observed from the table ELAA always provides results with no leakage dissipation, but at the cost of higher schedule length. The LBHS2D provides a good compromise between schedule length and leakage, and low leakage in most of the cases. Therefore, based on the requirements to trade between leakage and performance, one can employ LBHS2D to achieve good values for leakage dissipation and schedule length.

VI. CONCLUSION

In this work, we presented a heuristic approach to tackle the leakage power minimization problem on two dimensional re-configurable FPGAs. The proposed LBHS2D approach includes a leakage aware priority function at the scheduling stage and cost function with farthest placement scheme at the placement stage. The experimental results indicate effectiveness of the proposed approach. We can also see from the results that further improvement of the approaches is possible. In the future, we plan to explore on post placement adjustment of the approach to further reduce the leakage power consumption by taking fixed schedule length.

REFERENCES


Table I: Leakage waste and scheduled length for real-life applications

<table>
<thead>
<tr>
<th>Application</th>
<th>Performance</th>
<th>PDA</th>
<th>LBHS2D</th>
<th>ELAA</th>
<th>NAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>JPEG</td>
<td>Scheduled Length</td>
<td>23</td>
<td>22</td>
<td>25</td>
<td>28</td>
</tr>
<tr>
<td></td>
<td>Leakage dissipation</td>
<td>3</td>
<td>2</td>
<td>0</td>
<td>16</td>
</tr>
<tr>
<td>MPEG4</td>
<td>Scheduled Length</td>
<td>37</td>
<td>47</td>
<td>47</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td>Leakage dissipation</td>
<td>25</td>
<td>0</td>
<td>0</td>
<td>37</td>
</tr>
<tr>
<td>MP3</td>
<td>Scheduled Length</td>
<td>44</td>
<td>53</td>
<td>53</td>
<td>59</td>
</tr>
<tr>
<td></td>
<td>Leakage dissipation</td>
<td>30</td>
<td>1</td>
<td>0</td>
<td>40</td>
</tr>
</tbody>
</table>