flexMEDiC: flexible Memory Error Detection by Combined data encoding and duplication

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Motivation

- Frequency of transient HW faults (aka. soft errors) is increasing.
  - Traditional cause of faults: cosmic rays.
  - Vulnerability is increasing due to smaller feature sizes and lower operating voltages.
  - Dark/dim silicon in memory modules:
    - Extended refresh cycles for DRAM.
    - Lower supply voltage for SRAM.

- Limitations of ECC memory modules.
  - Typically SEC-DED codes (single error correction, double error detection).
  - Large fractions of memory errors cannot be handled by SEC-DED codes (Hwang et al., ASPLOS 2012).

Software-implemented error detection can be flexibly adjusted to detect complex (multi-bit) error patterns as well.
The simple **AN encoding** scheme is capable of detecting multi-bit errors:

- Fix an integer constant $A$.

- Encode integer values by multiplying by $A$:
  \[ n_{enc} = n \times A \]

- Decode by dividing by $A$:
  \[ n = \frac{n_{enc}}{A} \]

- Check for errors:
  \[ n_{enc} \mod A = 0 \]

- Error-detecting capability varies with the constant $A$.
  - Powers of 2 are ill-suited to error detection.
  - $A = 58659$ is known to have good properties; can detect up to 5 bit flips, Hoffmann et al., 2015.

- AN encoding introduces large overheads if used to protect operations: several $10x$-$100x$. 

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Detection of multiple bit errors in memory, including caches, load-store queues.

Apply AN encoding only to values stored to memory → low overhead due to AN encoding.

encode before storing:
\[
\begin{align*}
%0 &= \text{mul i64} \%0, \ A \\
\text{store i64} \%0, \text{164} \%p
\end{align*}
\]

check and decode after loading:
\[
\begin{align*}
%1 &= \text{load i64*} \%p \\
%2 &= \text{srem i64} \%1, \ A \\
&\quad \quad \quad \cdots \\
%3 &= \text{sdiv i64} \%2, \ A
\end{align*}
\]

AN encoding is applied at the LLVM IR level.
- Common approach in software-implemented fault tolerance schemes.

Error detection at the IR level misses memory accesses that are inserted by the compiler backend.

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flexMEDiC – cont’d

- Frequency of unprotected memory accesses (at the level of LLVM IR):

  - Two major sources of backend-inserted memory accesses: register spills, function calls.
  - Using DMR keeps function calls efficient.
  - DMR can detect arbitrarily many bit flips within the same data word.

Apply DMR to backend-inserted memory accesses:

- Frequency of unprotected memory accesses (at the level of LLVM IR):

  - Using DMR keeps function calls efficient.
  - DMR can detect arbitrarily many bit flips within the same data word.

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Full memory error detection

<table>
<thead>
<tr>
<th>letter</th>
<th>test case</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>array reduction</td>
</tr>
<tr>
<td>B</td>
<td>bubblesort</td>
</tr>
<tr>
<td>C</td>
<td>CRC-32</td>
</tr>
<tr>
<td>D</td>
<td>DES encryption</td>
</tr>
<tr>
<td>E</td>
<td>Dijkstra (shortest path)</td>
</tr>
<tr>
<td>F</td>
<td>expression evaluation</td>
</tr>
<tr>
<td>G</td>
<td>token lexer</td>
</tr>
<tr>
<td>H</td>
<td>expression parser</td>
</tr>
<tr>
<td>I</td>
<td>matrix multiplication</td>
</tr>
<tr>
<td>J</td>
<td>array copy</td>
</tr>
<tr>
<td>K</td>
<td>quicksort</td>
</tr>
<tr>
<td>L</td>
<td>switch</td>
</tr>
</tbody>
</table>

*) sampled 0.01% of all possible error patterns within a single data word.

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**Runtime overhead**

**Geometric means across test programs***:**

- **Overhead due to DMR only***:

<table>
<thead>
<tr>
<th>DMR</th>
<th>overhead</th>
</tr>
</thead>
<tbody>
<tr>
<td>frame pointer</td>
<td>1.020</td>
</tr>
<tr>
<td>callee-saved register</td>
<td>1.009</td>
</tr>
<tr>
<td>jump tables</td>
<td>1.013</td>
</tr>
<tr>
<td>return address</td>
<td>1.027</td>
</tr>
<tr>
<td>function arguments</td>
<td>1.005</td>
</tr>
<tr>
<td>register spills</td>
<td>1.012</td>
</tr>
<tr>
<td>all</td>
<td>1.073</td>
</tr>
</tbody>
</table>

*) runtime measurements performed on 64-bit Intel Core i7, at 3.6GHz

- **Total runtime overhead due to flexMEDiC** is 1.55x.
- **AN encoding** introduces an overhead of only about 1.4x.
- **DMR measures** inserted by the compiler backend introduce an overhead of only 1.07x.
- Memory overhead of AN encoding is $\log(A)$ bits per data word.
- Memory overhead of DMR is 100%, but used sparingly.
flexMEDiC can successfully **detect multi-bit errors** in memory.

The number of detectable bits can be adjusted flexibly by varying the encoding constant A.
- Finding appropriate A is a fundamental problem in AN encoding.

flexMEDiC relies on DMR only for local memory accesses → applicable to multi-threaded applications with shared memory.

What hardware support can one think of to efficiently support the memory overhead of AN encoding of \( \log(A) \)?

Have observed similar distributions of program responses to varying numbers of bit flips.
- Is there a fundamental reason for this (e.g. due to the nature of certain programs)?
- How can one capitalize on this for the purpose of software-implemented fault tolerance?
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Thank you.